

4.5.1 – 168 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:

- 64 BIT without PARITY
- 72 BIT for PARITY CODES
- 72 BIT & 80 BIT for ECC CODES

CONFIGURATION—21 Different Configurations are defined using various combinations of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.

LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" features that consist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.1-A, 4.5.1-B, & 4.5.1-C

CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.5.1-D

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.1-E through 4.5.1-AB

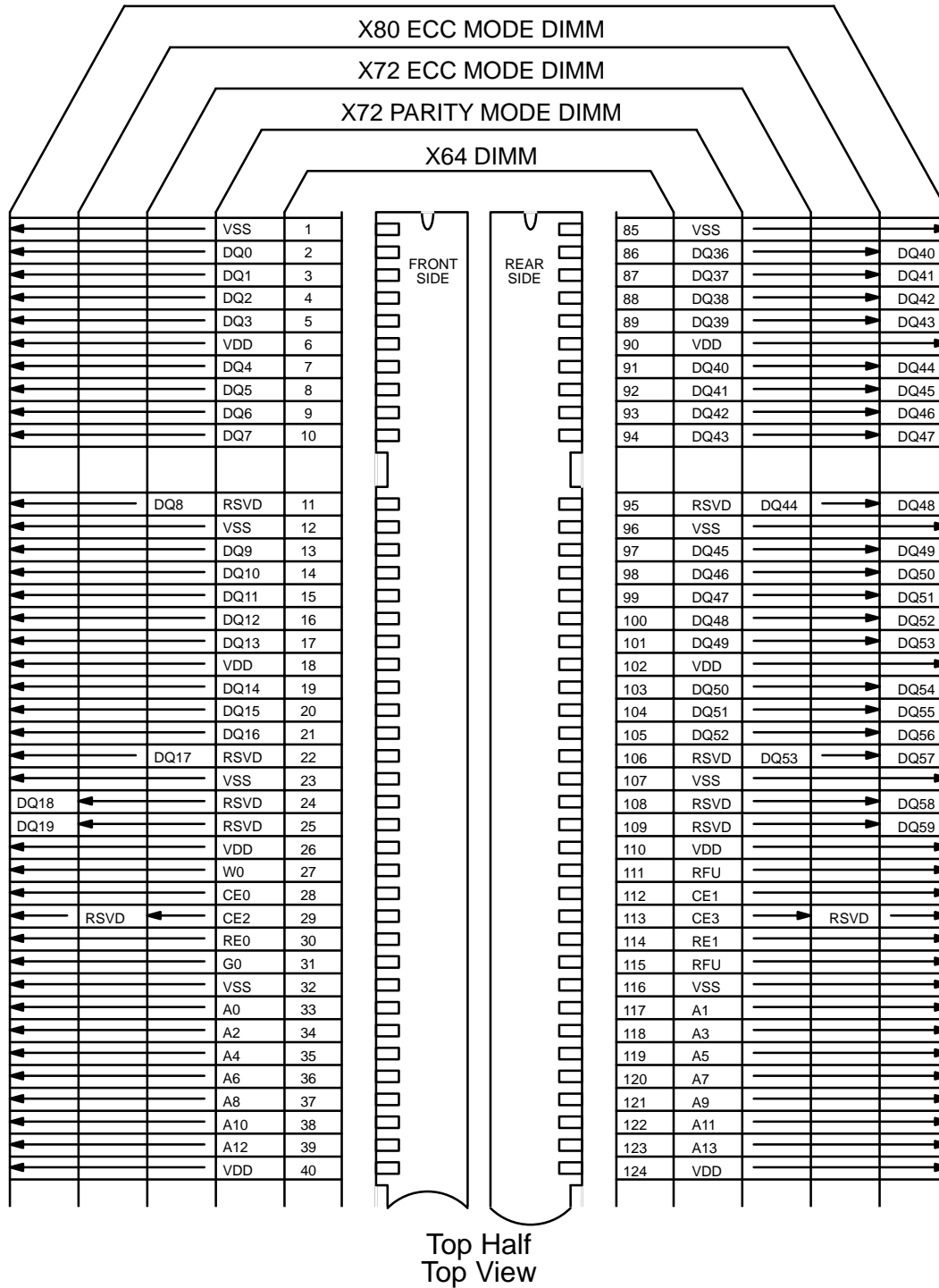
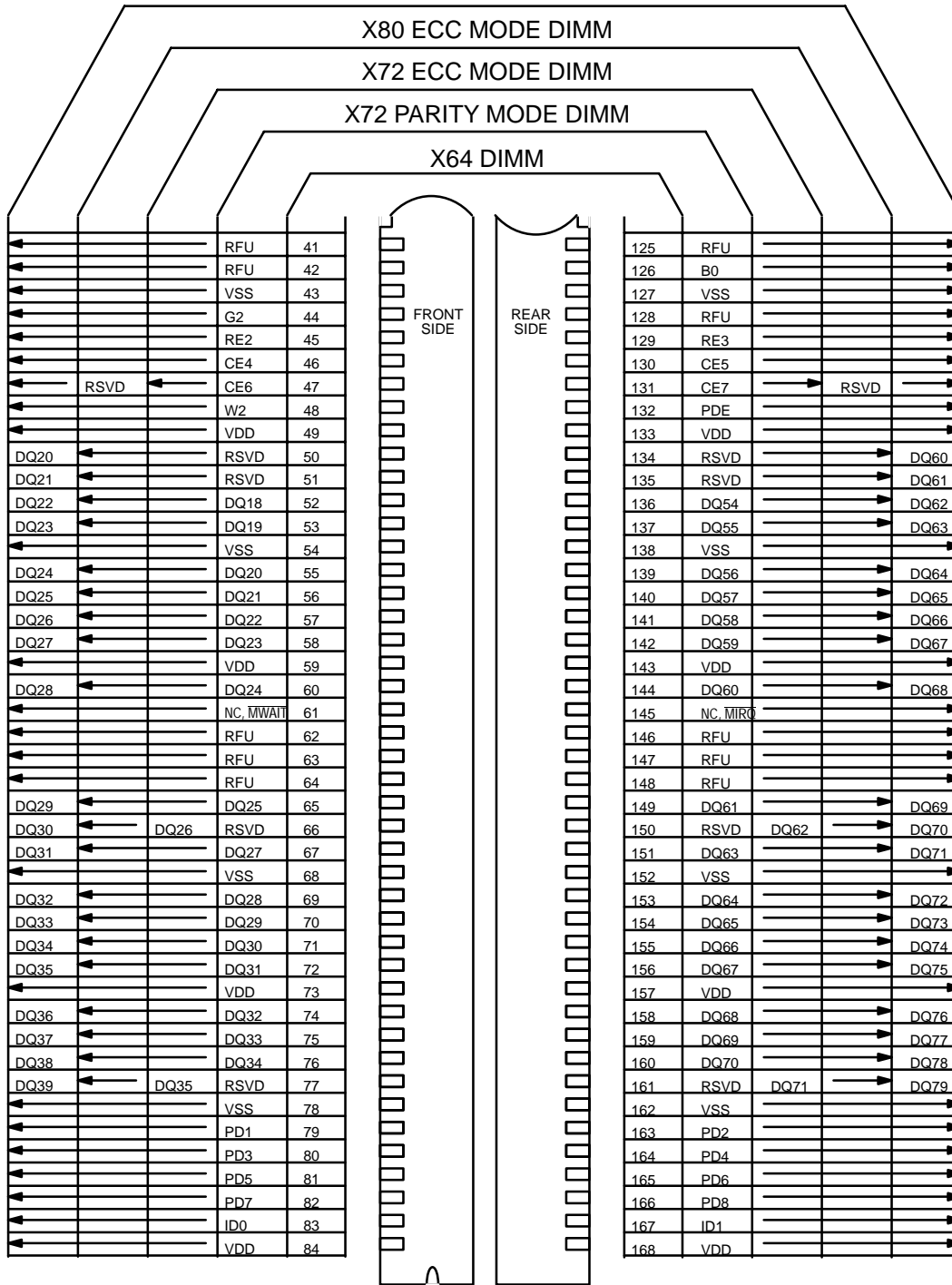


Figure 4.5.1-A
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, TOP HALF



Bottom Half
Top View

Figure 4.5.1-B
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

JEDEC Standard No. 21-C

Page 4.5.1-4

PD 4	PD 3	PD 2	PD 1	DIMM CONFIGURATION (Parity, ECC)	# BANKS	DRAM CONFIGURATION	DRAM ROW ADDR	DRAM COL. ADDR	Av. REFRESH INTERVAL (μS)	
									NORMAL	SLOW
0	0	0	0	256K X 64/72, 72	1	256K X 16/18	9	9	15.6	125
0	0	0	1	512K X 64/72, 72	2	256K X 16/18	9	9	15.6	125
0	0	1	0	512K X 64/72, 72/80	1	512K X 8/9	10	9	15.6	125
0	0	1	1	1M X 64/72, 72/80	2	512K X 8/9	10	9	15.6	125
0	1	0	0	1M X 64/72, 72/80	1	1M X 4/16/18	10	10#	15.6	125
0	1	0	1	2M X 64/72, 72/80	2	1M X 4/16/18	10	10#	15.6	125
0	1	1	0	1M X 64/72, 72	1	1M X 16/18	12	8	15.6	31.2
1	0	0	0	2M X 64/72, 72	2	1M X 16/18	12	8	15.6	31.2
1	0	0	1	2M X 64/72, 72/80	1	2M X 8	11	10	15.6	62.5
1	0	1	0	4M X 64/72, 72/80	2	2M X 8	11	10	15.6	62.5
1	0	1	1	4M X 72	1	4M X 1/4	12**	11**	15.6	31.2
1	0	1	1	4M X 64, 72/80	1	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	0	8M X 64/72, 72/80	2	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	1	8M X 64/72, 72/80	1	8M X 8	12	11	15.6	31.2
1	1	1	0	16M X 64/72, 72/80	2	8M X 8	12	11	15.6	31.2
1	1	1	1	16M X 64/72, 72/80	1	16M X 4	13/12	11/12	15.6	TBD/31.2
0	0	0	0	16M X 64/72, 72	1	16M X 16	13/12	11/12	15.6	TBD/31.2
0	0	0	1	32M X 64/72, 72/80	2	16M X 4/16	13/12	11/12	15.6	TBD/31.2
0	0	1	0	32M X 64/72, 72/80	1	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	0	1	1	64M X 64/72, 72/80	2	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	1	0	0	64M X 64/72, 72/80	1	64M X 4	14/13	12/13	7.8/15.6	TBD*
0	1	1	1	Expansion						

Note 1) * These modules using 256M devices are for reference only and will be further defined in the future.

Note 2) 1 = Logic high ; 0 = Logic low; In Table Information.

Note 3) ** This addressing includes a redundant address to allow mixing of 12/10(X4) and 11/11(X1) DRAMs

Note 4) # 1M X 16/18 DRAMS with 10/10 addressing may dissipate excessive power in many applications. Care must be taken to ensure device thermal limits are not exceeded. 12/8 addressing is provided as a lower power option.

PD Note: PD & ID terminals must each be pulled up through a resistor to VDD at the next higher level assembly.

PDs will either be open or driven to VOH or driven to VOL via on-board buffer circuits.

ID Note: IDs will either be open (NC) or connected directly to VSS without a buffer.

	PD7	PD6
SPEED (tRAC)	82	165
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

	PD8	ID0
CONFIGURATION	166	83
X64	1	0
X72 PARITY	1	1
X72 ECC	0	0
X80 ECC	0	1
DATA CONFIGURATION		

	ID1
REFRESH MODE	167
NORMAL	0
SELF-REFRESH	1
REFRESH MODE	

	PD5
DATA ACCESS MODE	81
FAST PAGE	0
FP W/EDO	1
EDO DETECTION	

Figure 4.5.1-C

168 PIN, 64, 72, or 80 BIT DIMM PRESENCE DETECT & CONFIGURATION TABLES

64, 72, & 80 BIT DRAM DIMM CAPACITY IN M BYTE																				
Memory Device DIMM Configuration	4M DRAM					16M DRAM					64M DRAM					256M DRAM				
	256K		512K		1M	1M		2M		4M	4M		8M		16M	16M		32M		64M
	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4
256K X 64		4																		
256K X 72	4																			
256K X 72 (ECC)	4																			
256K X 80 (ECC)																				
512 X 64		8		8																
512K X 72	8		8																	
512K X 72 (ECC)	8		8	9																
512K X 80 (ECC)				10																
1M X 64				16	16		4													
1M X 72			16		18	4														
1M X 72 (ECC)			16	18	18	4														
1M X 80 (ECC)				20	20															
2M X 64						8		8												
2M X 72					8		8													
2M X 72 (ECC)					8		8	9												
2M X 80 (ECC)								10												
4M X 64								16	16		4									
4M X 72							16		18	4										
4M X 72 (ECC)							16	18	18	4										
4M X 80 (ECC)								20	20											
8M X 64											8		8							
8M X 72										8		8								
8M X 72 (ECC)										8		8	9							
8M X 80 (ECC)													10							
16M X 64													16	16		4				
16M X 72													16	18	4					
16M X 72 (ECC)													16	18	18	4				
16M X 80 (ECC)														20	20					
32M X 64																8		8		
32M X 72															8		8			
32M X 72 (ECC)															8		8	9		
32M X 80 (ECC)																		10		
64M X 64																			16	16
64M X 72																		16		18
64M X 72 (ECC)																		16	18	18
64M X 80 (ECC)																			20	20

Figure 4.5.1–D

168 PIN, 64, 72, & 80 BIT DRAM DIMM Capacity Table

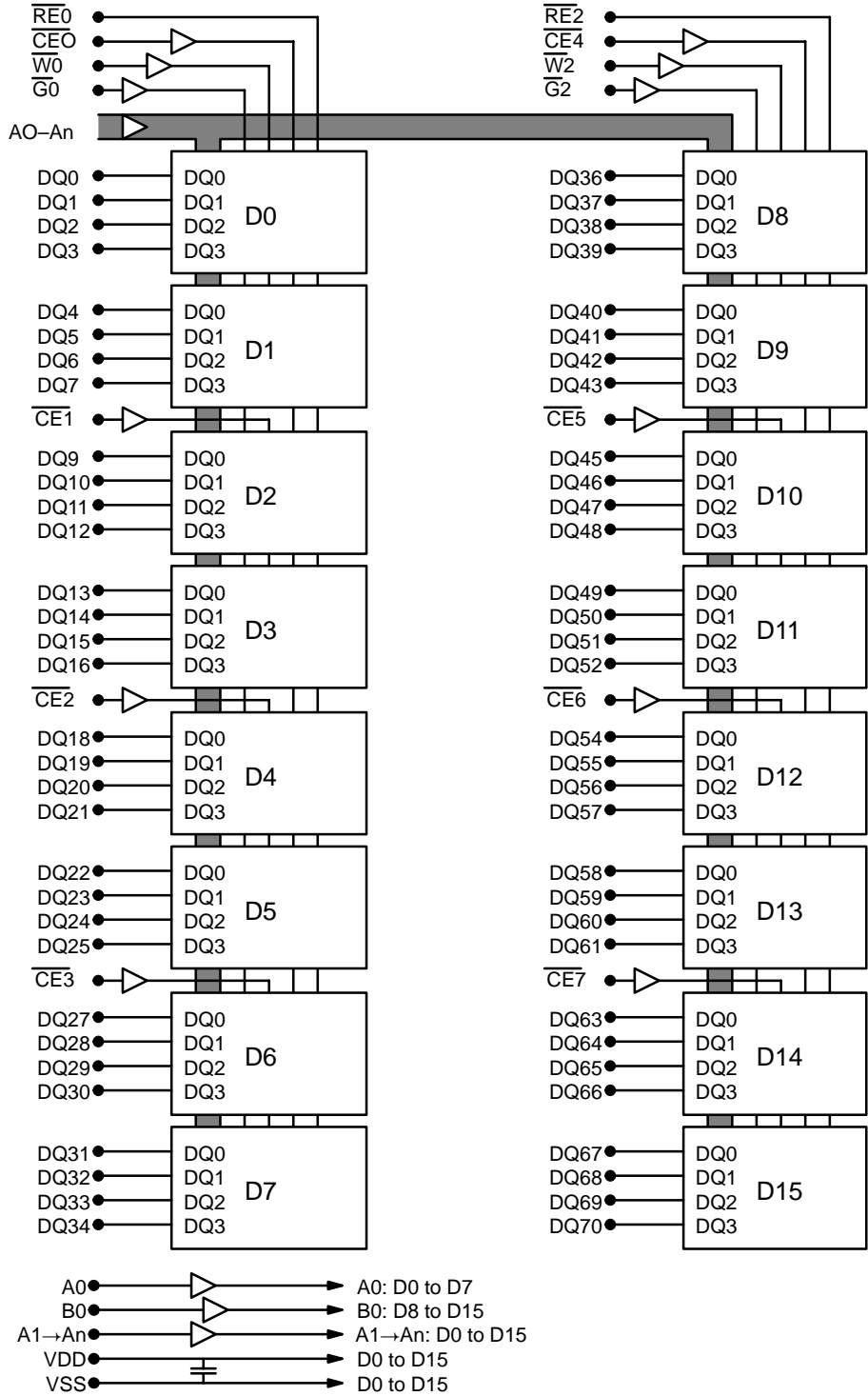


Figure 4.5.1-E
168 PIN, X64 DRAM DIMM, 1 bank with X4 DRAMs

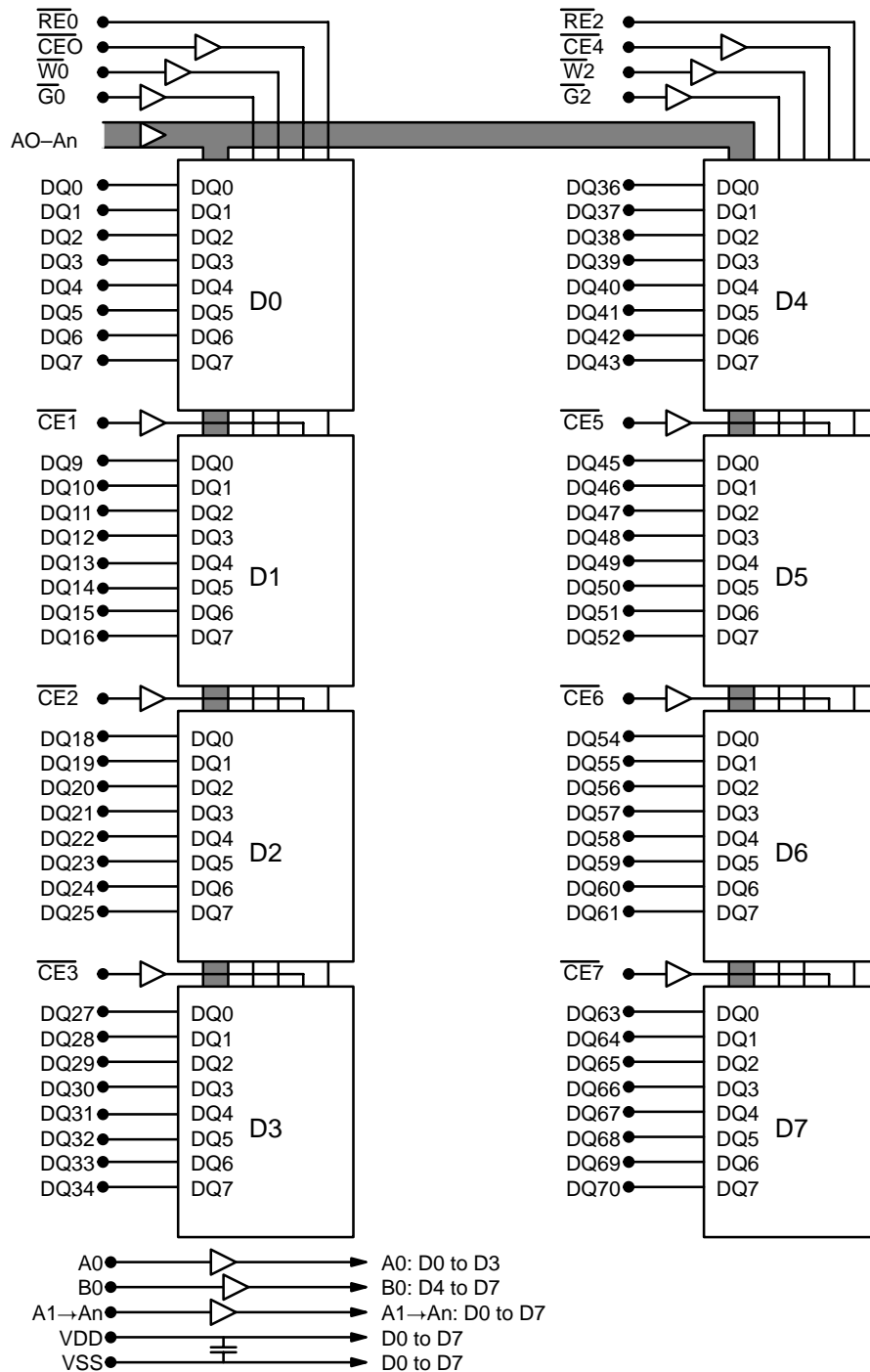


Figure 4.5.1-F
168 PIN, X64 DRAM DIMM, 1 bank with X8 DRAMs

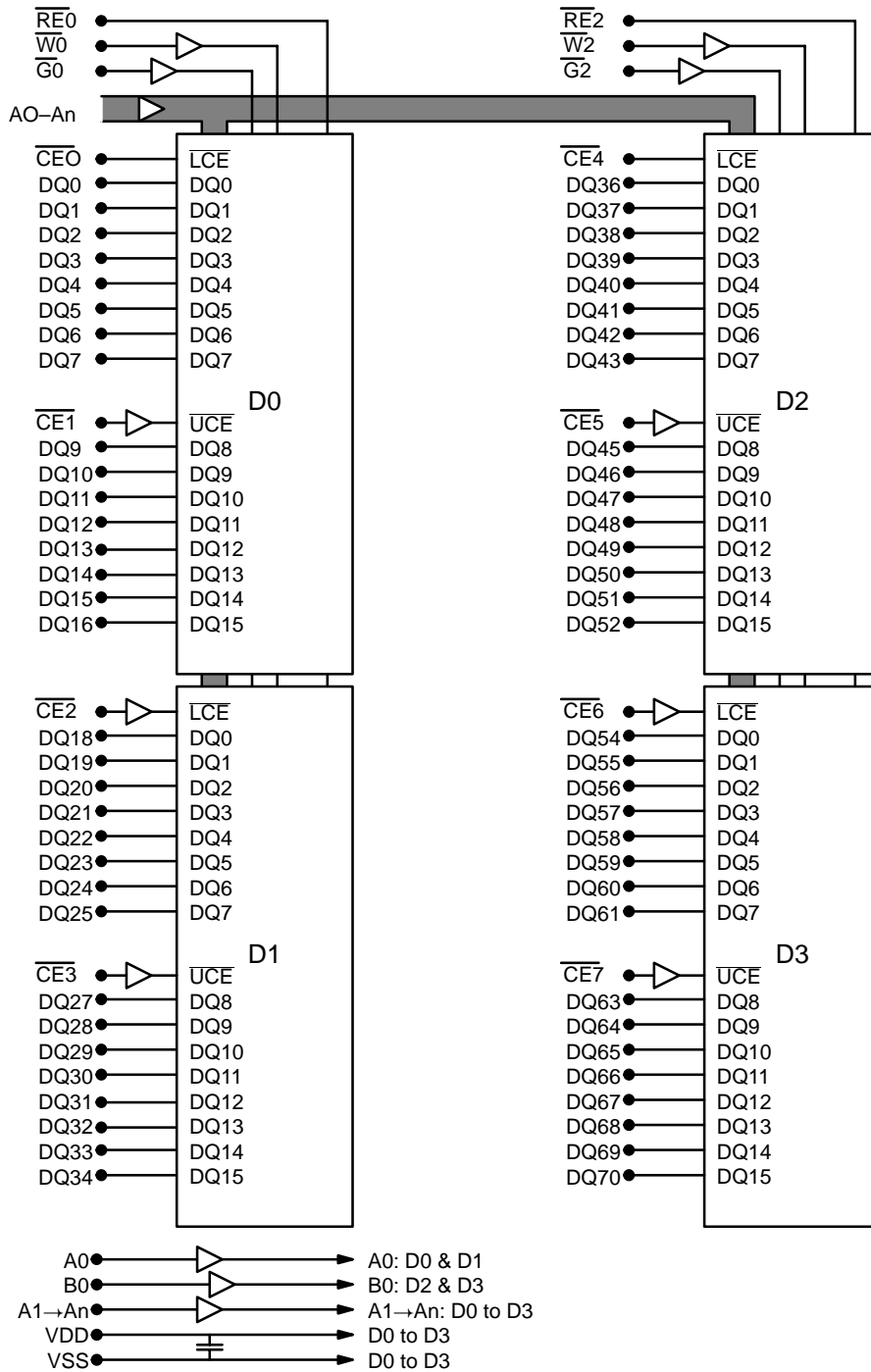


Figure 4.5.1-G
168 PIN, X64 DRAM DIMM, 1 bank with X16 DRAMs

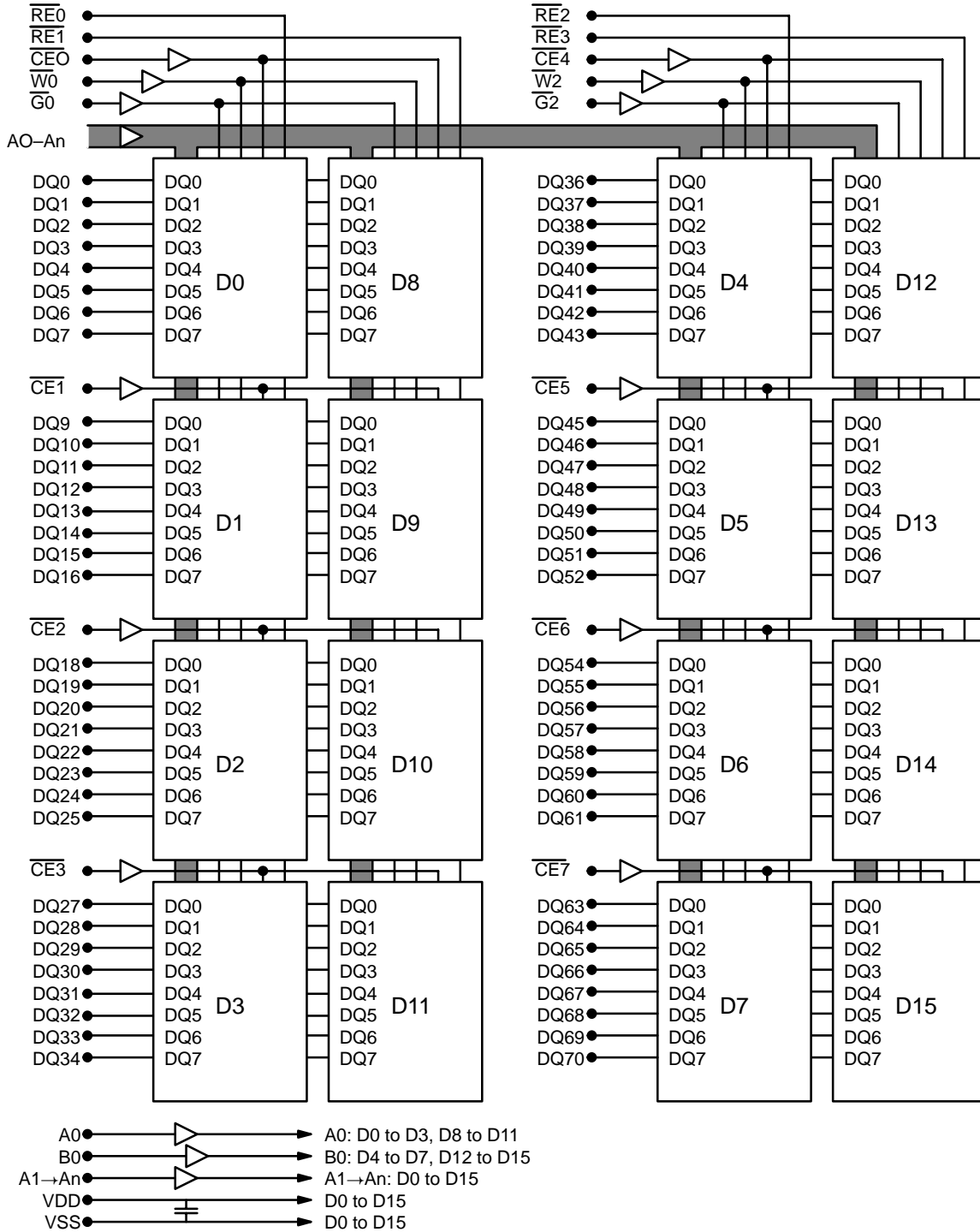


Figure 4.5.1-H

168 PIN, X64 DRAM DIMM, 2 banks with X8 DRAMs

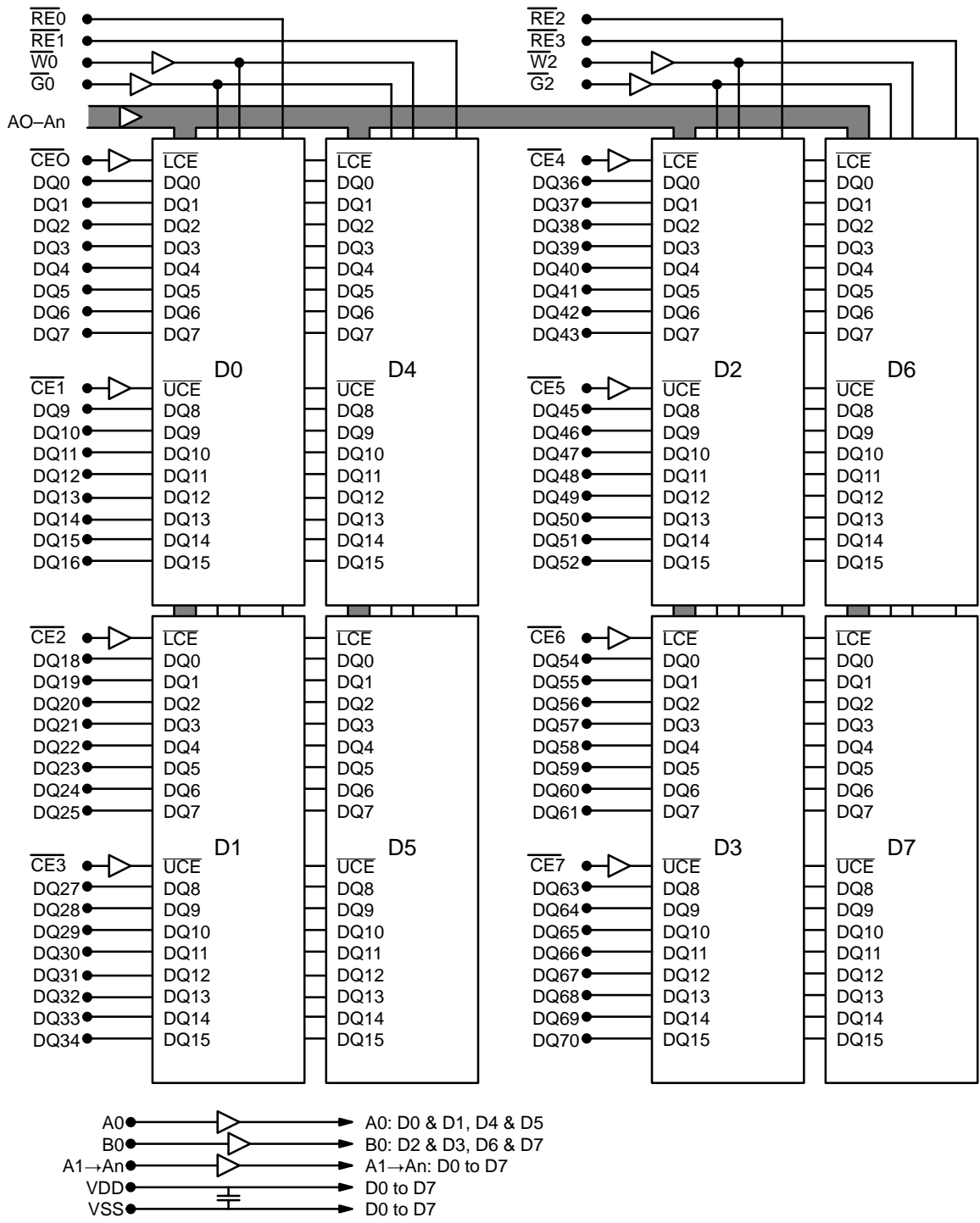


Figure 4.5.1-1
168 PIN, X64 DRAM DIMM, 2 banks with X16 DRAMs

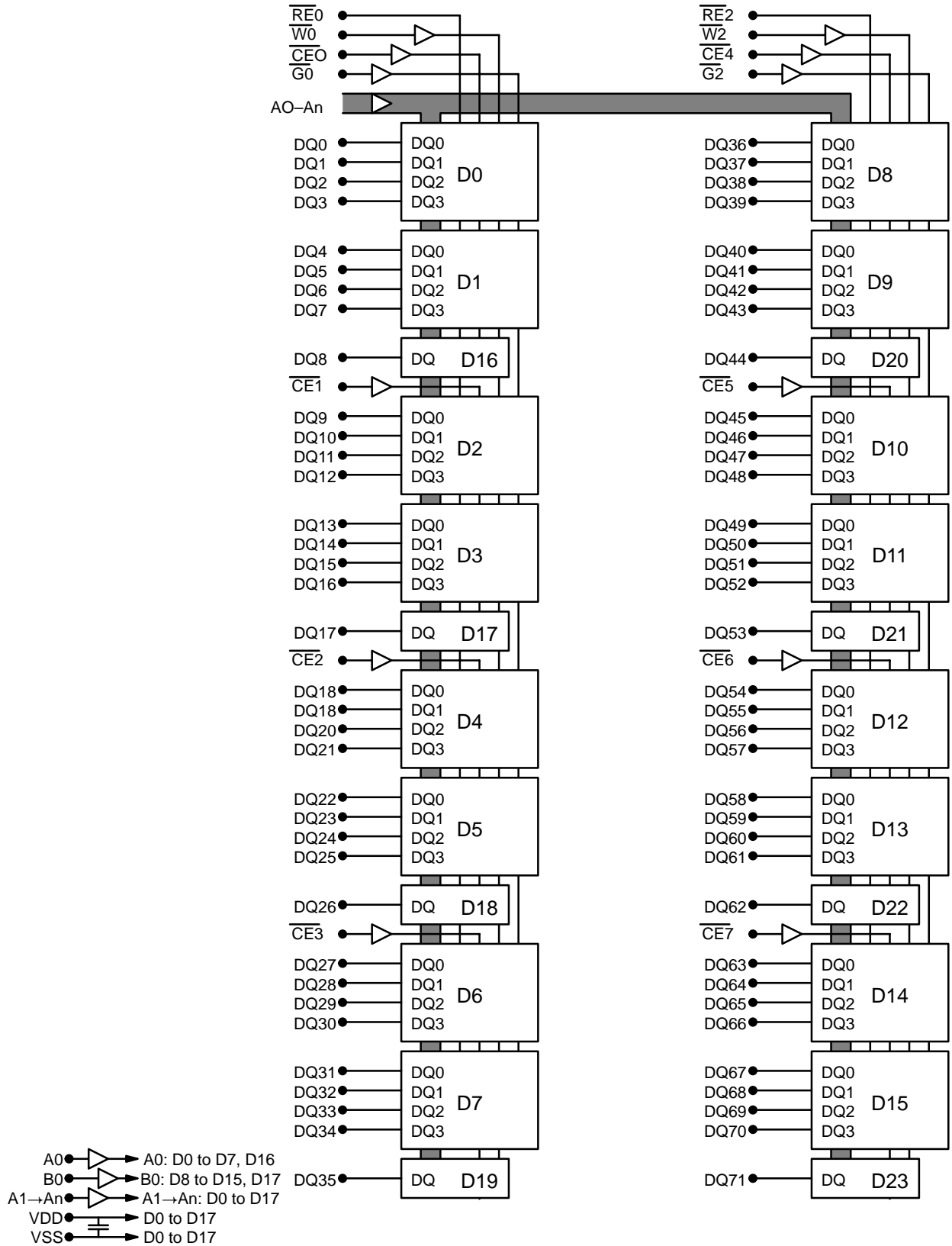


Figure 4.5.1-J

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X1 DRAMs
Release 4c7

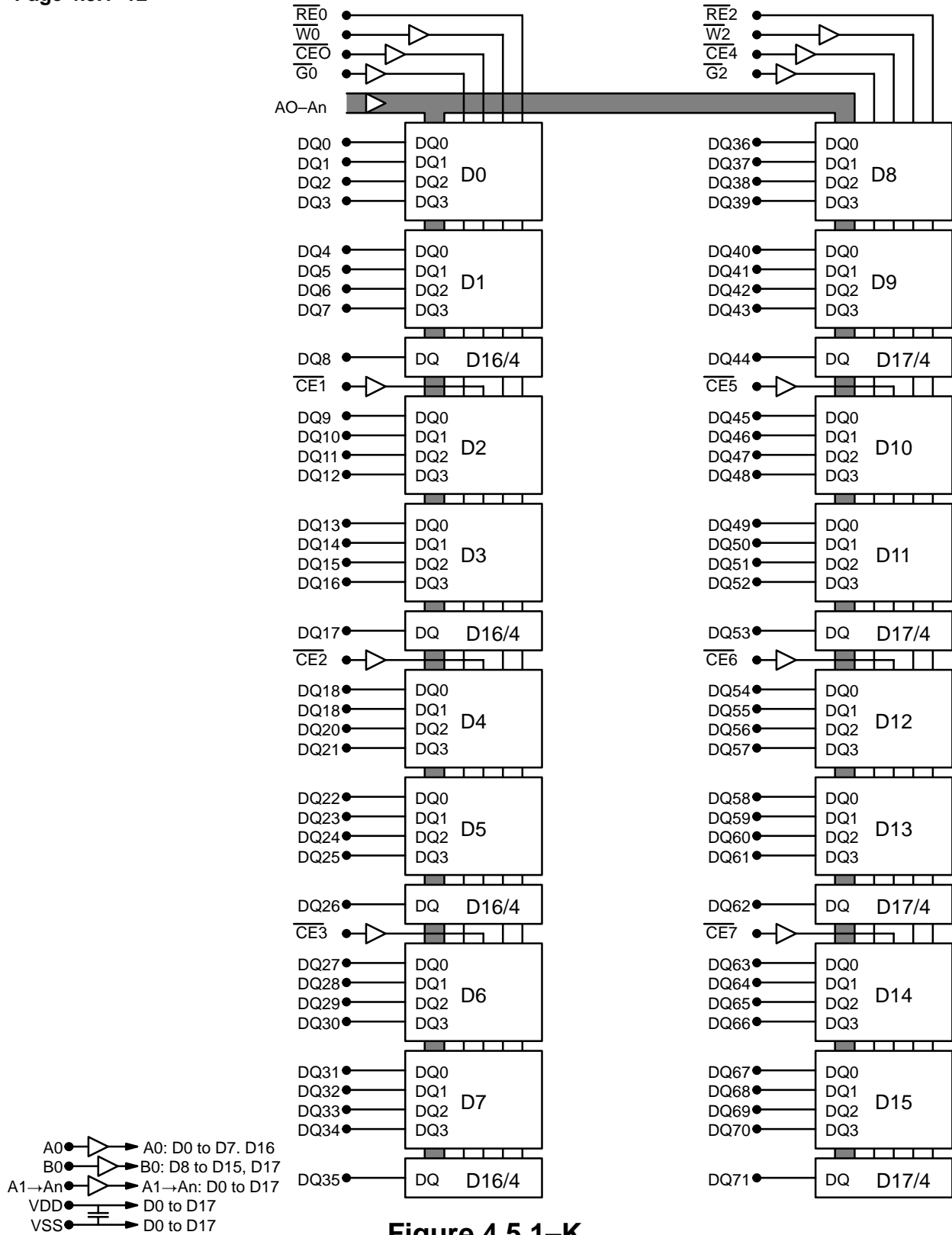


Figure 4.5.1-K

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X4 W/4 CE DRAMs

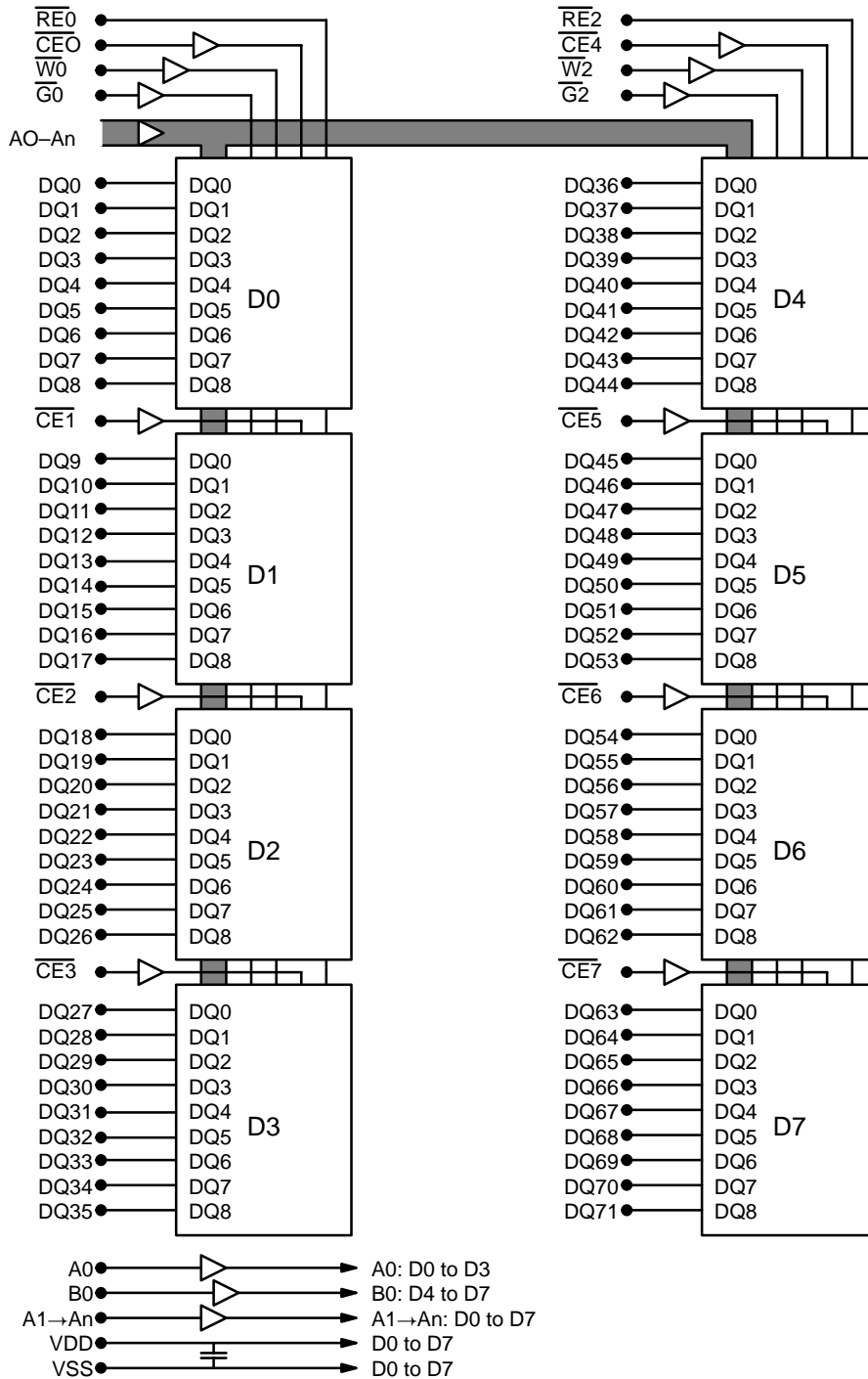


Figure 4.5.1-L

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X9 DRAMs
Release 4-7

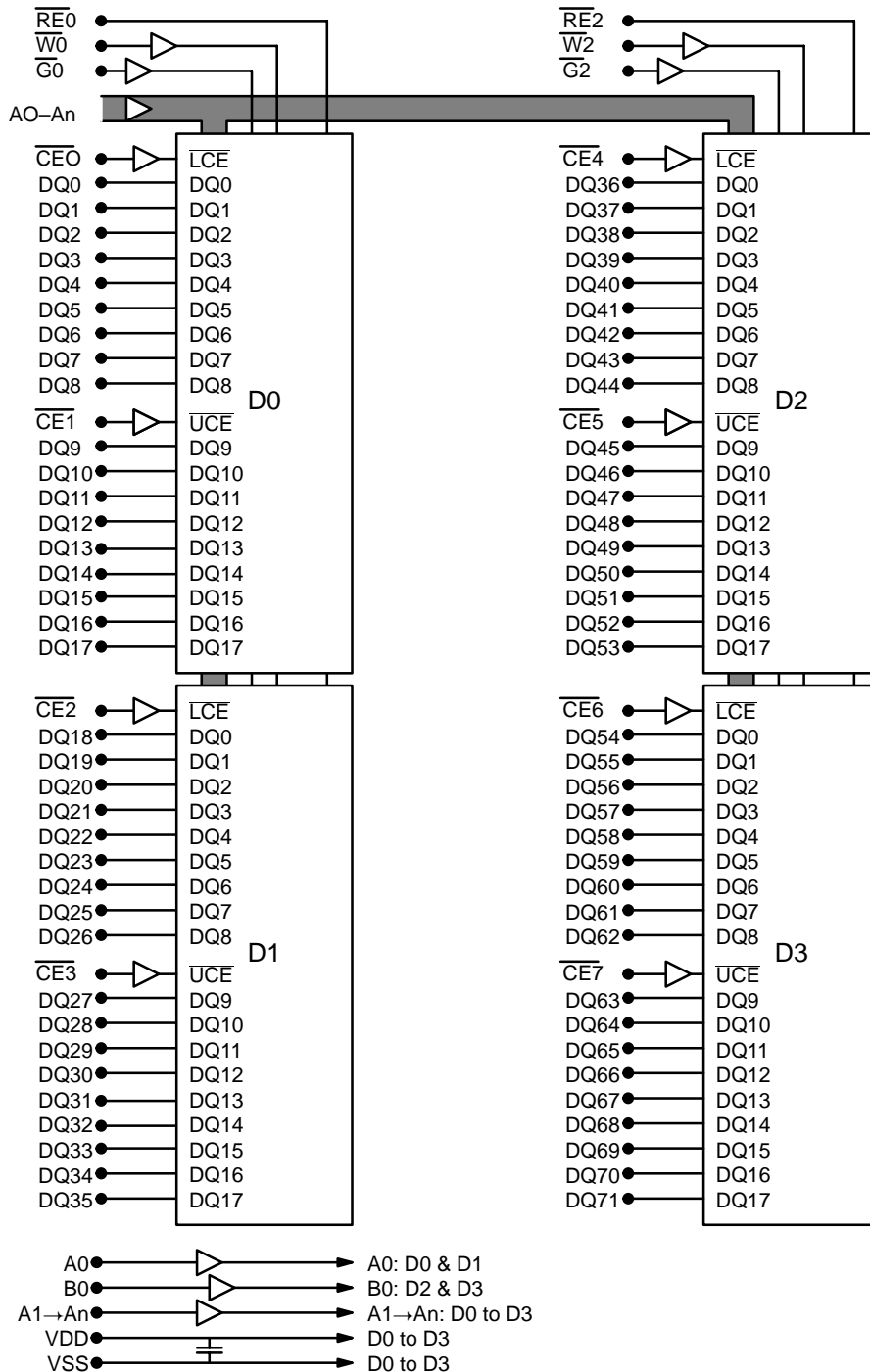


Figure 4.5.1-M
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X18 DRAMs

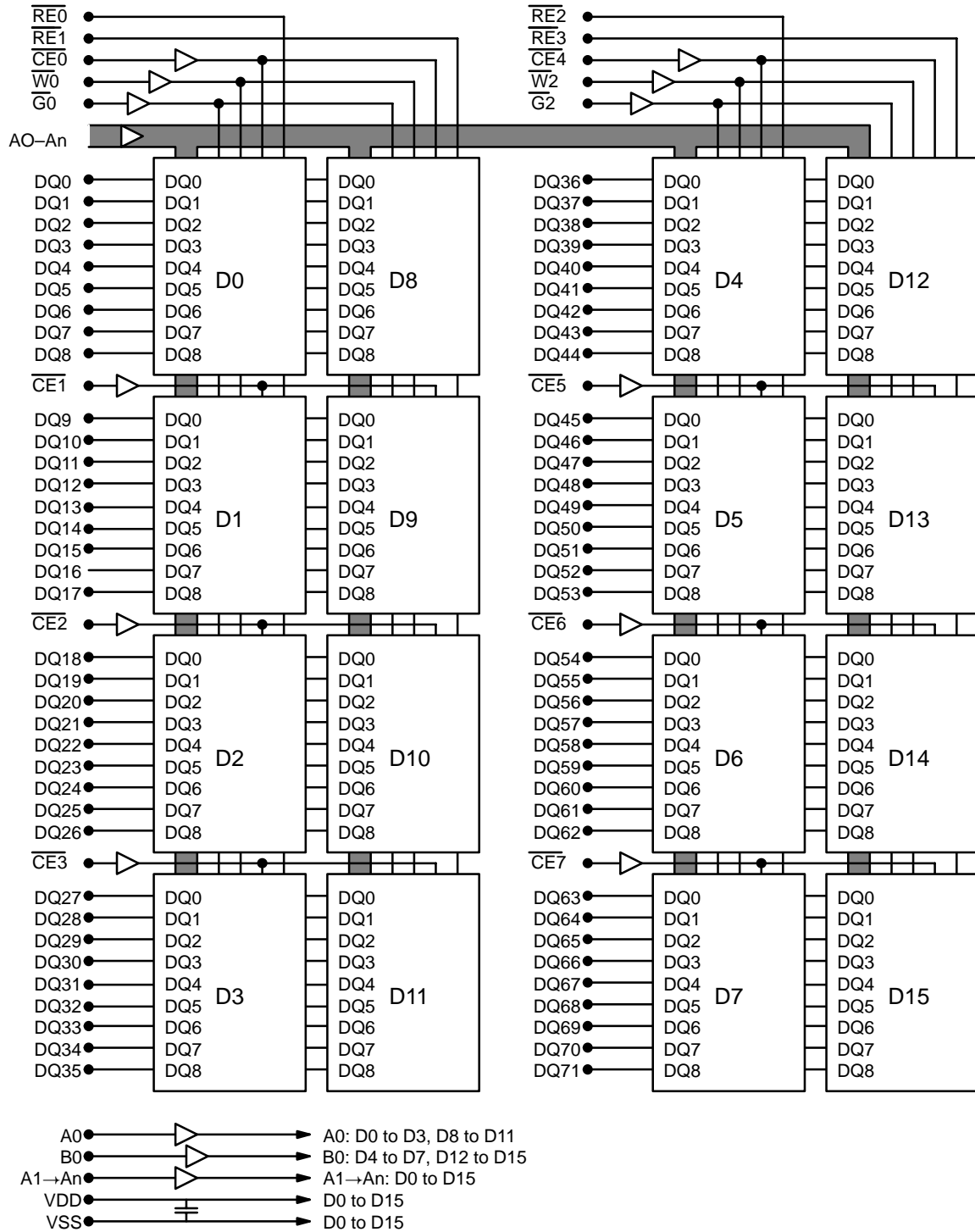


Figure 4.5.1-N
168 PIN, X72 (Parity mode) DRAM DIMM, 2 banks with X9 DRAMs
Release 4-7

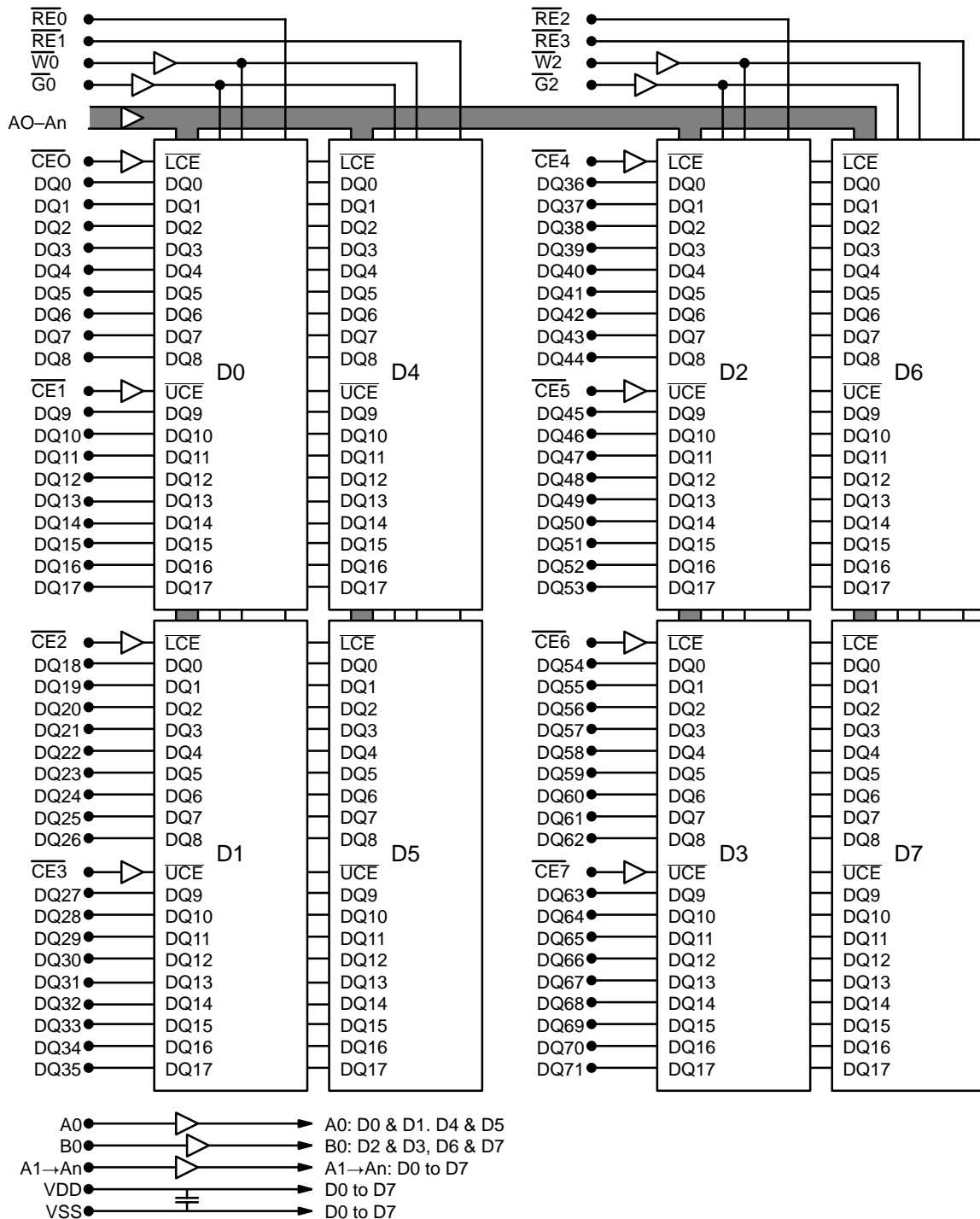


Figure 4.5.1-O
168 PIN, X72 (Parity mode) DRAM DIMM, 2 bank with X18 DRAMs

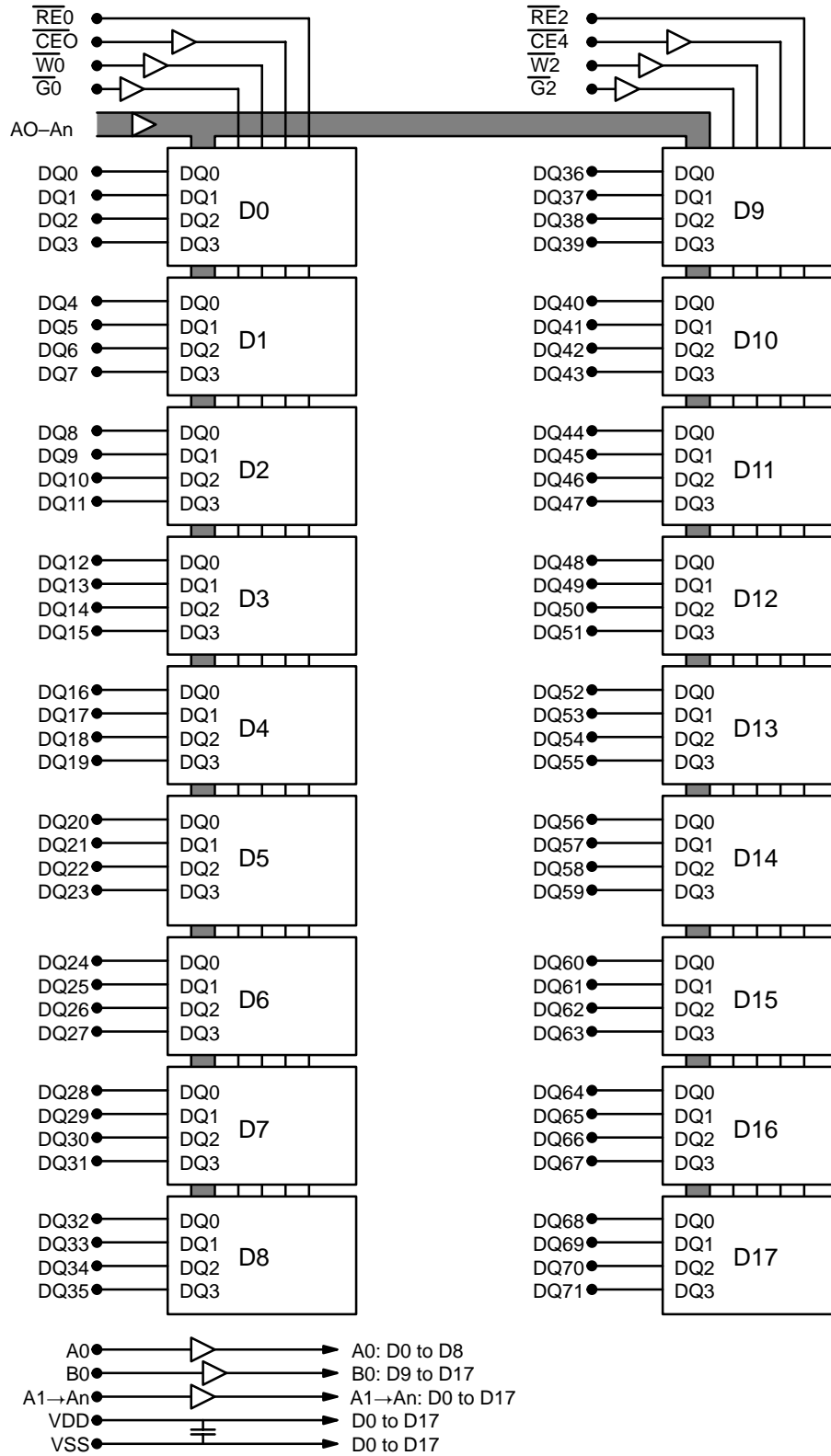
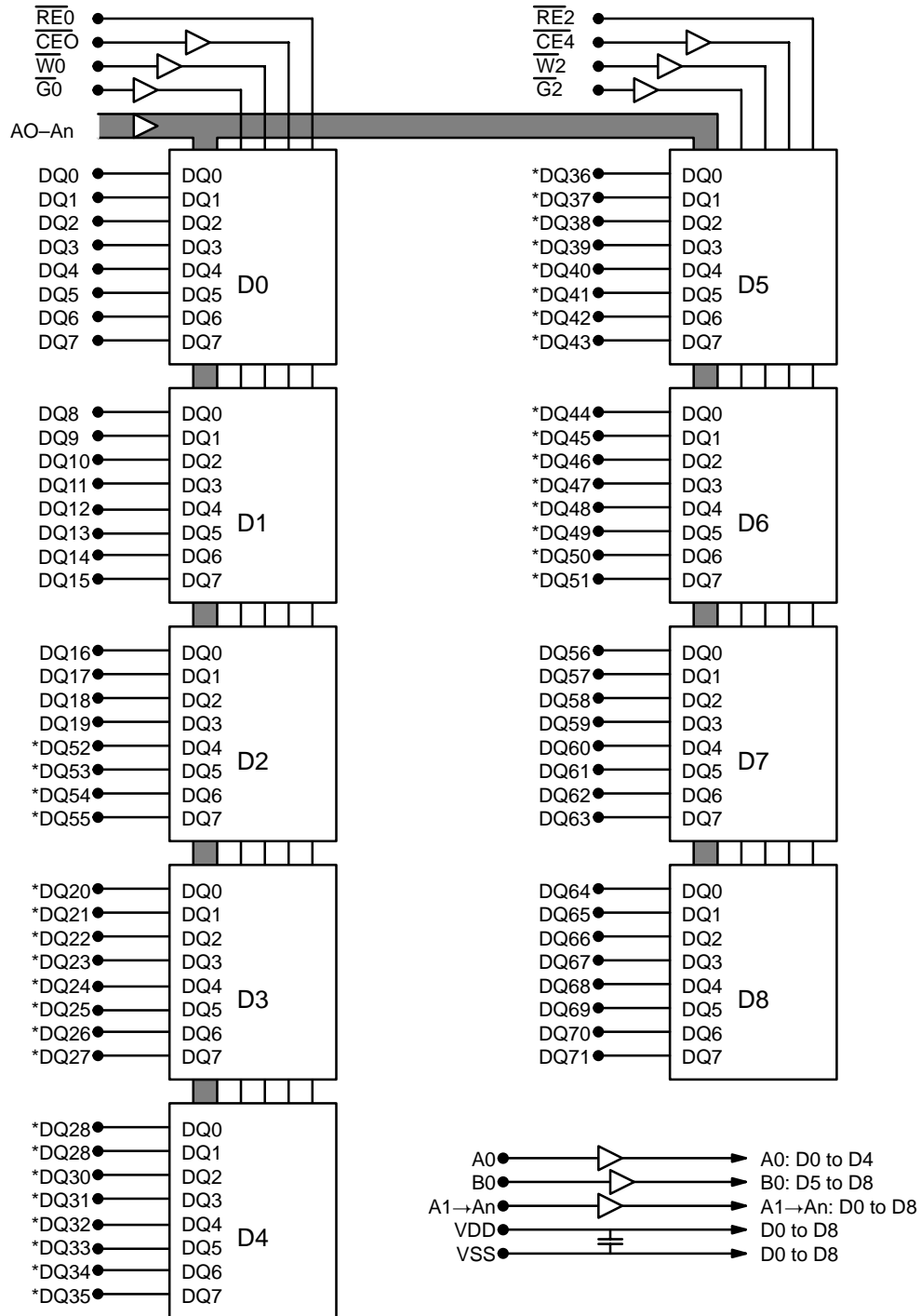


Figure 4.5.1-P

168 PIN, X 72 (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs
Release 4c7



* Note: The location of data pins DQ-20 through DQ-55 have been changed in Release 7

Figure 4.5.1-Q
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs
Release 4-r7

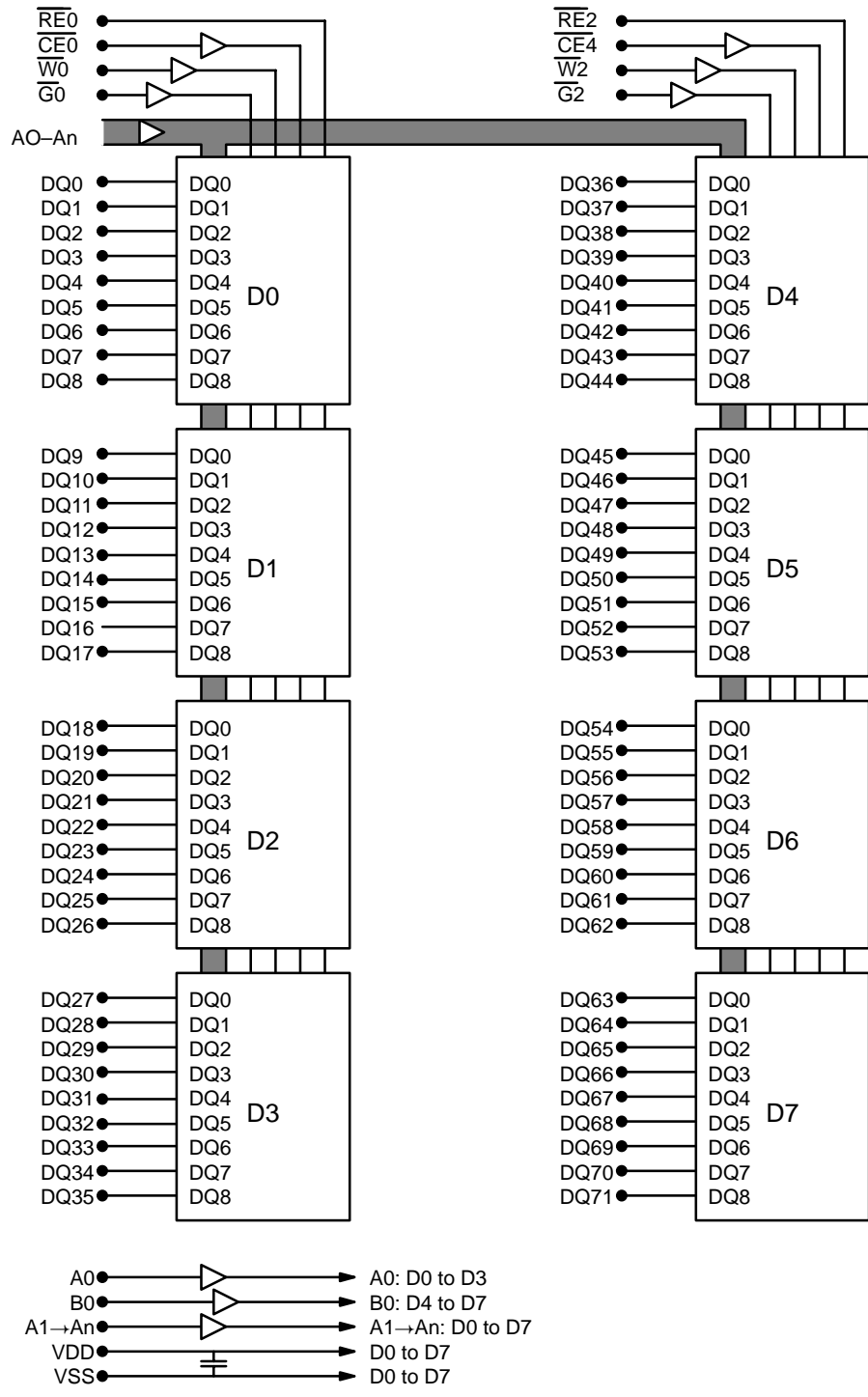


Figure 4.5.1-R
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X9 DRAMs
Release 4c7

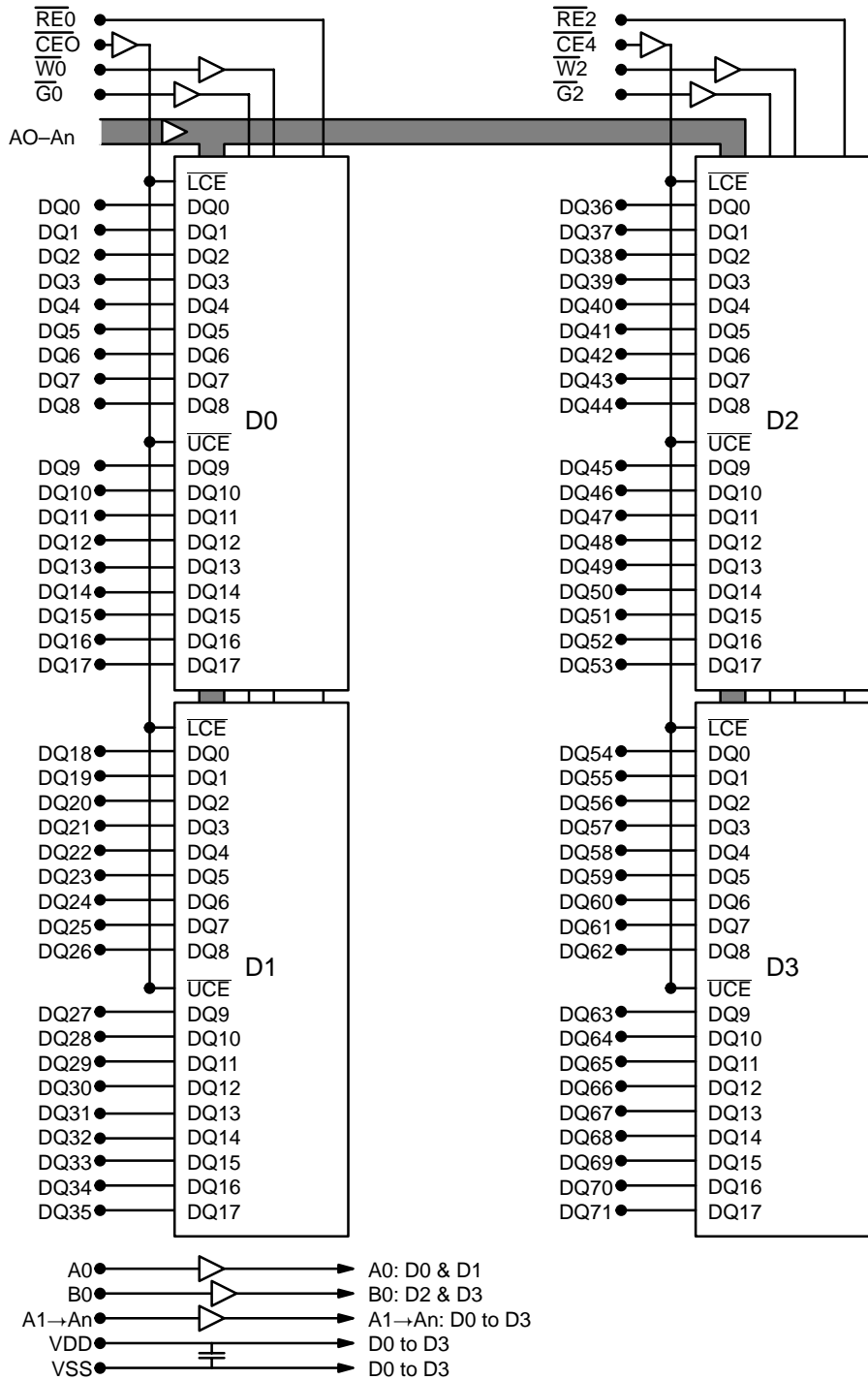


Figure 4.5.1-S
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X18 DRAMs

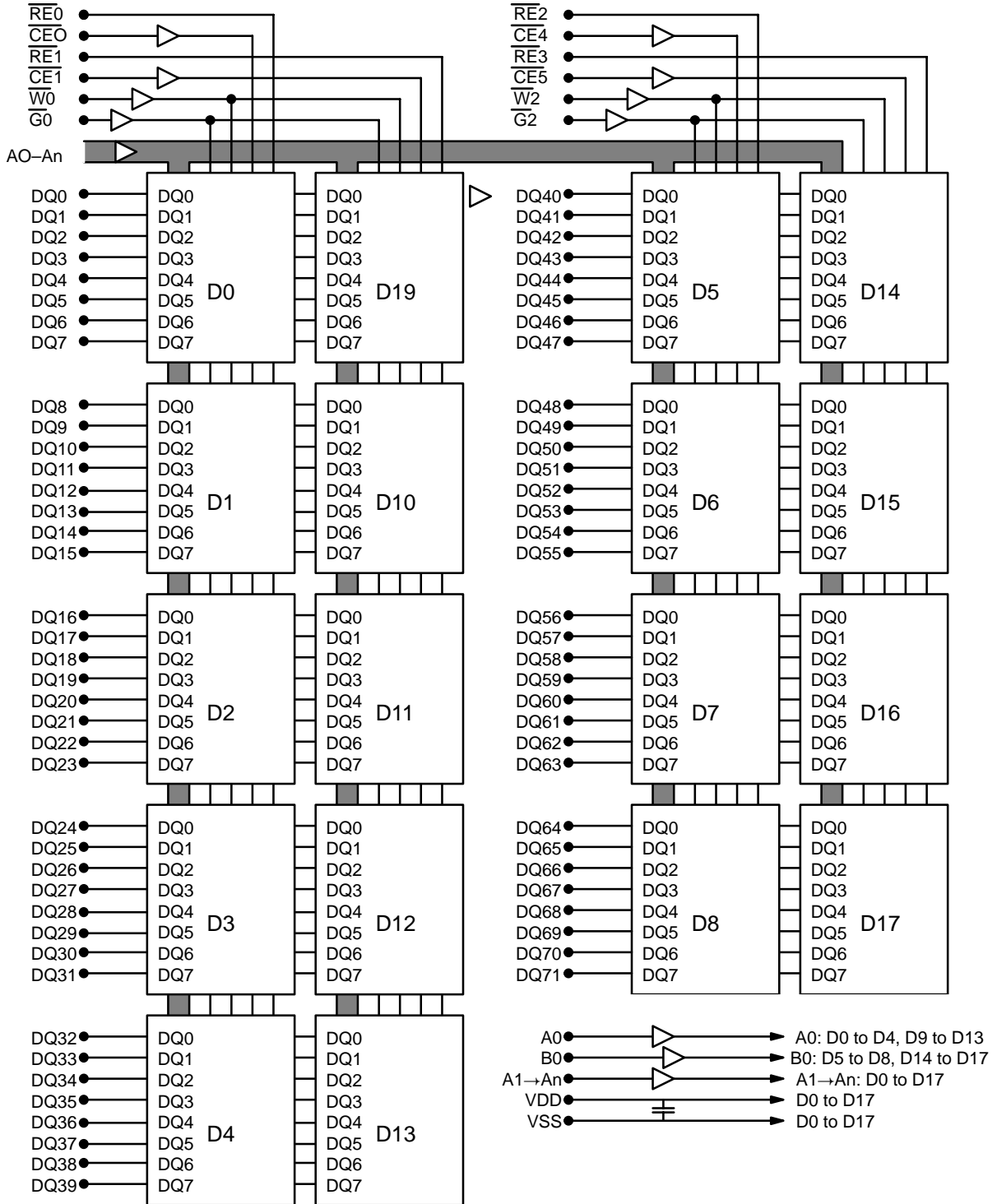


Figure 4.5.1-T

168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs
Release 4-7

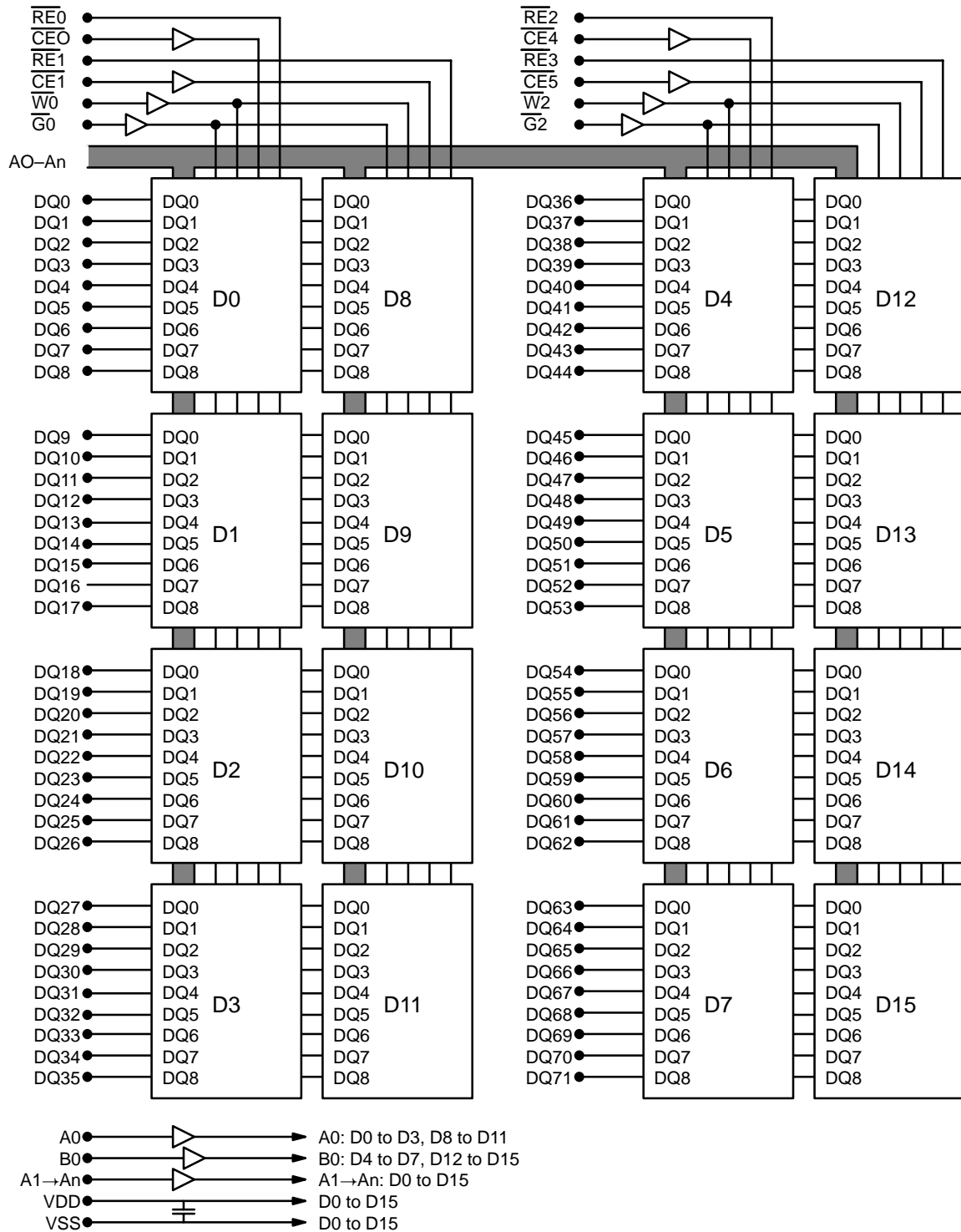


Figure 4.5.1-U
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X9 DRAMs
Release 4-7

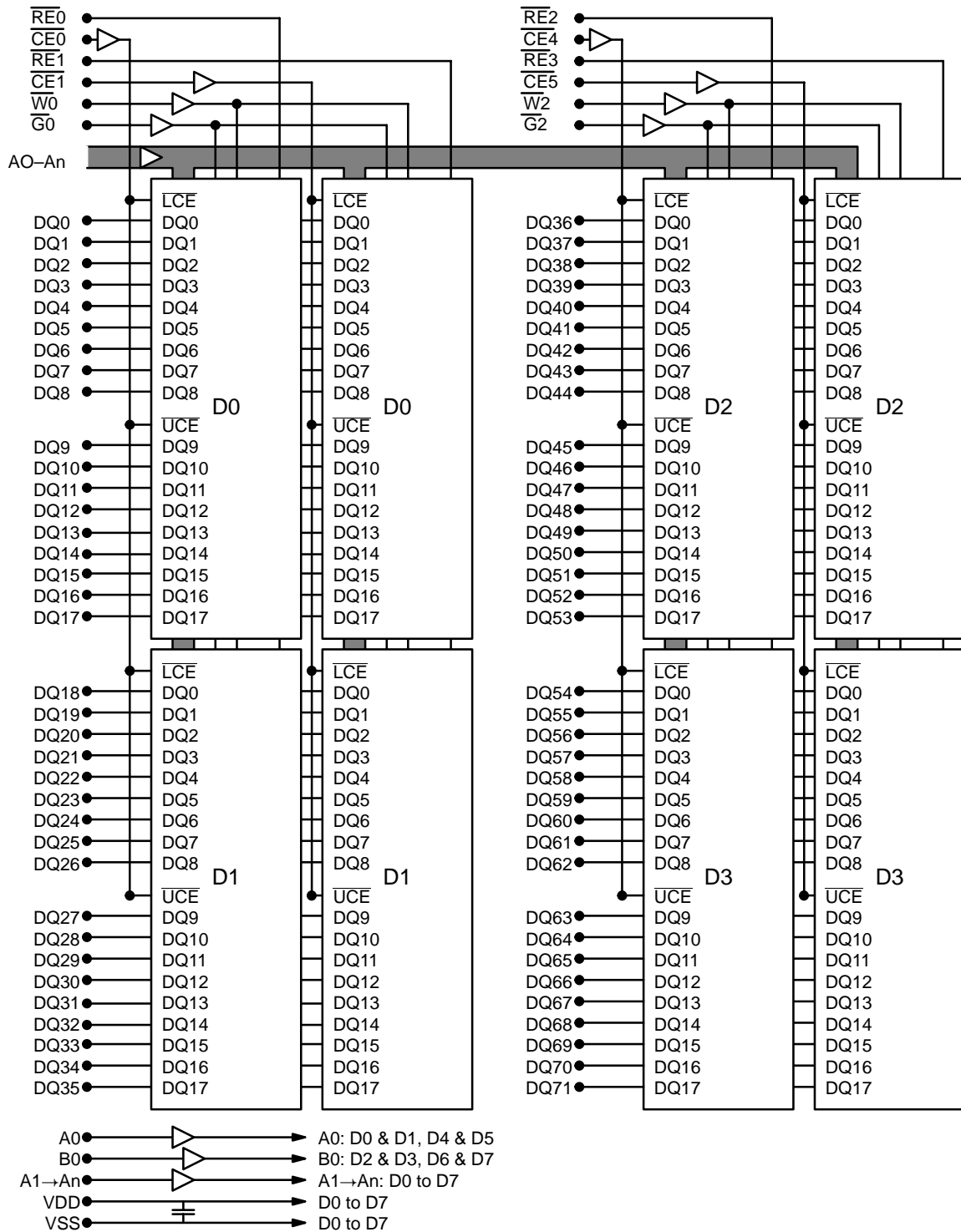


Figure 4.5.1-V

168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X18 DRAMs
Release 4-7

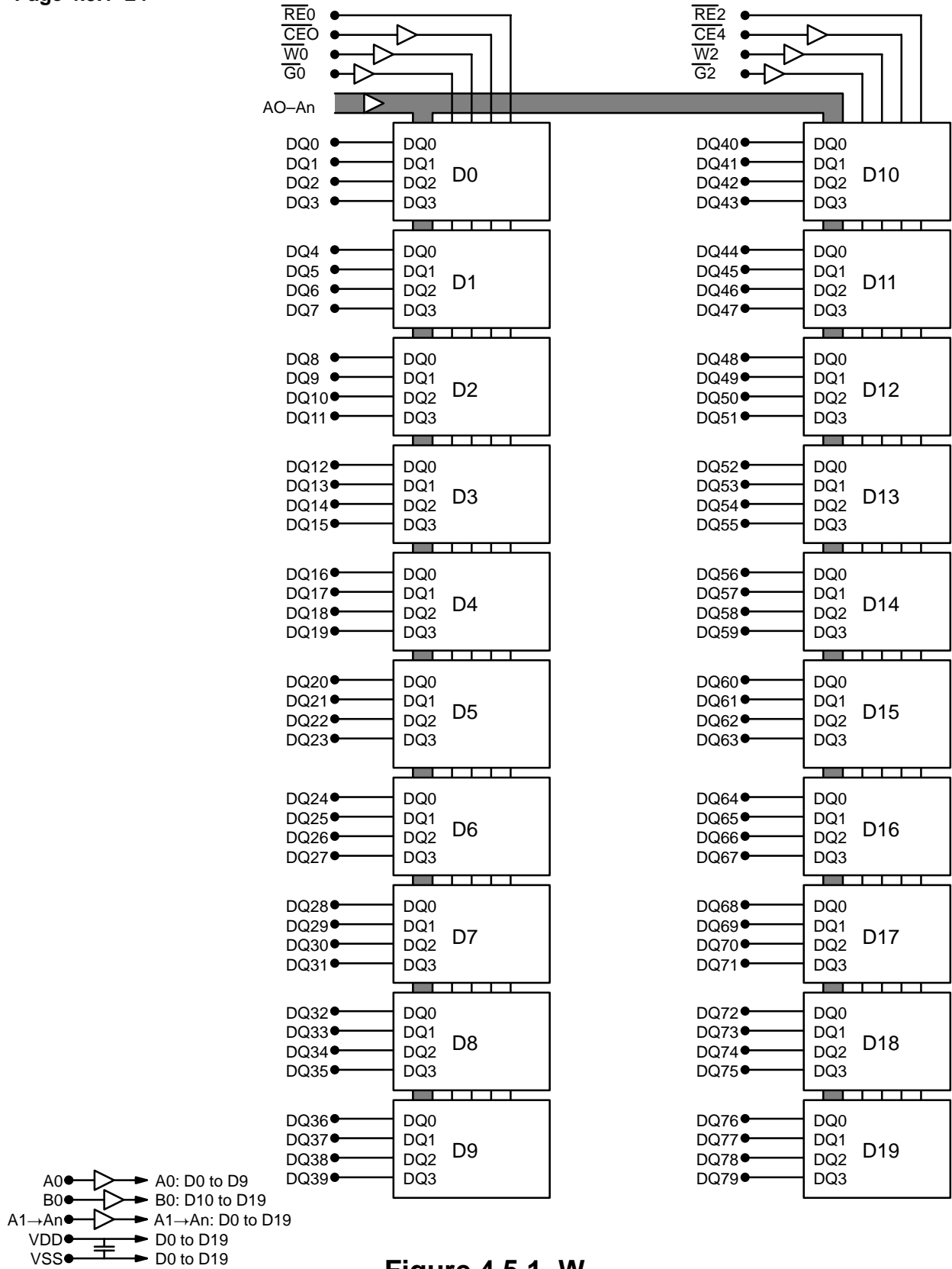


Figure 4.5.1-W

168 PIN, 80 BIT (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs

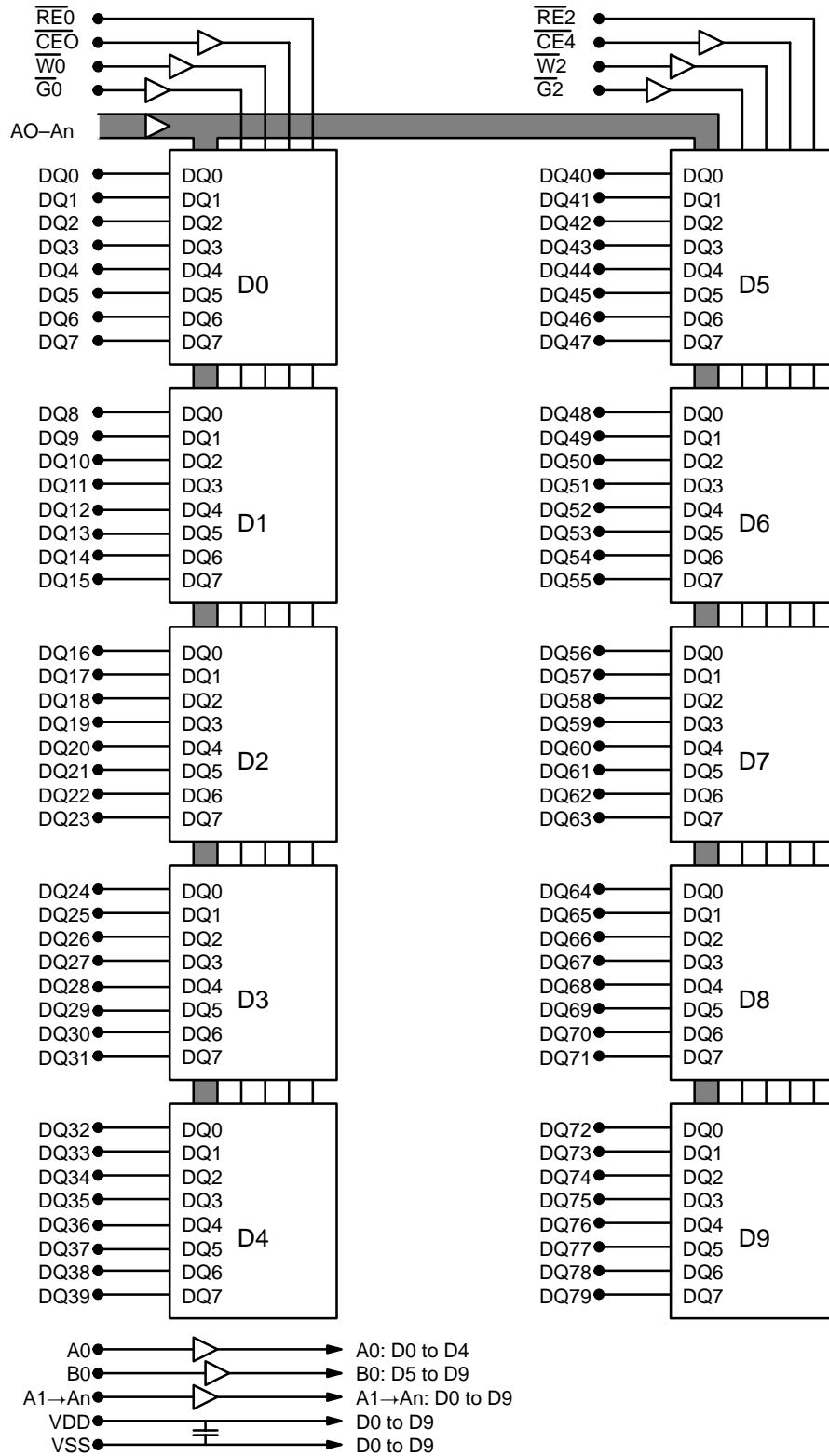


Figure 4.5.1-X

168 PIN, X80 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs
Release 4-7

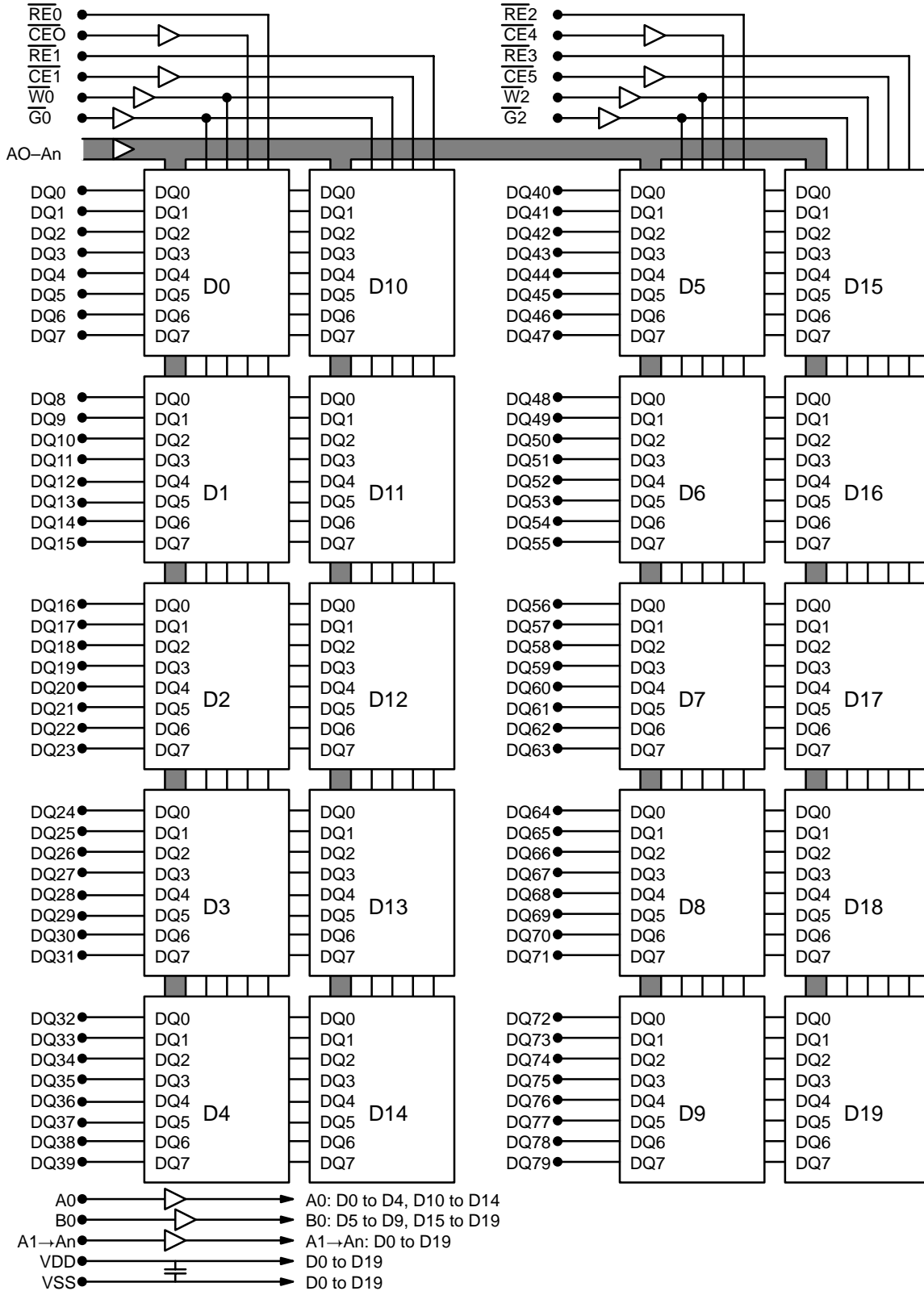


Figure 4.5.1-Y

168 PIN, X80 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

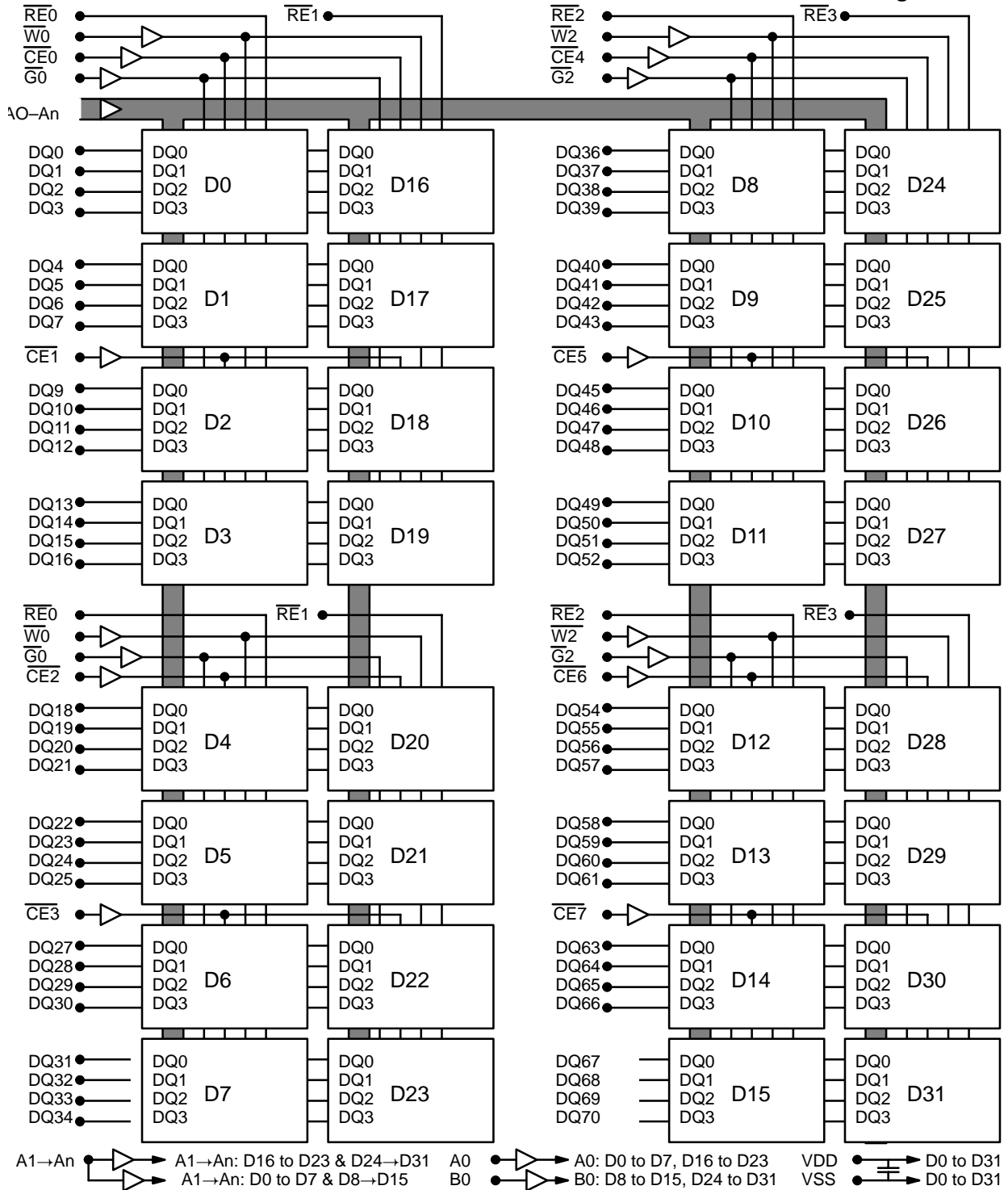


Figure 4.5.1-Z

168 PIN, X64 DRAM DIMM, 2 BANK with X4 DRAMs

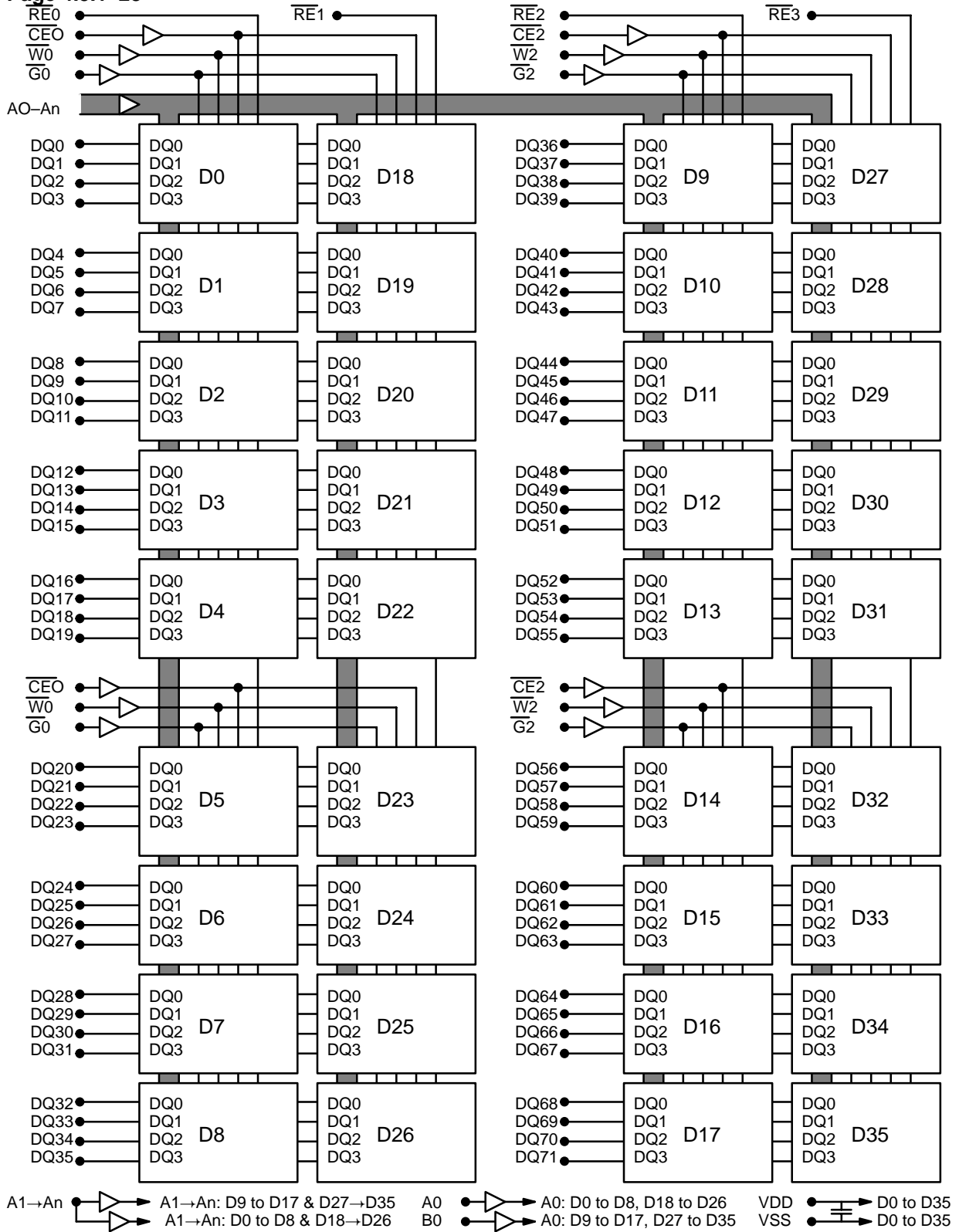


Figure 4.5.1-AA
168 PIN, X72 ECC DRAM DIMM, 2 BANK, X4 DRAMs

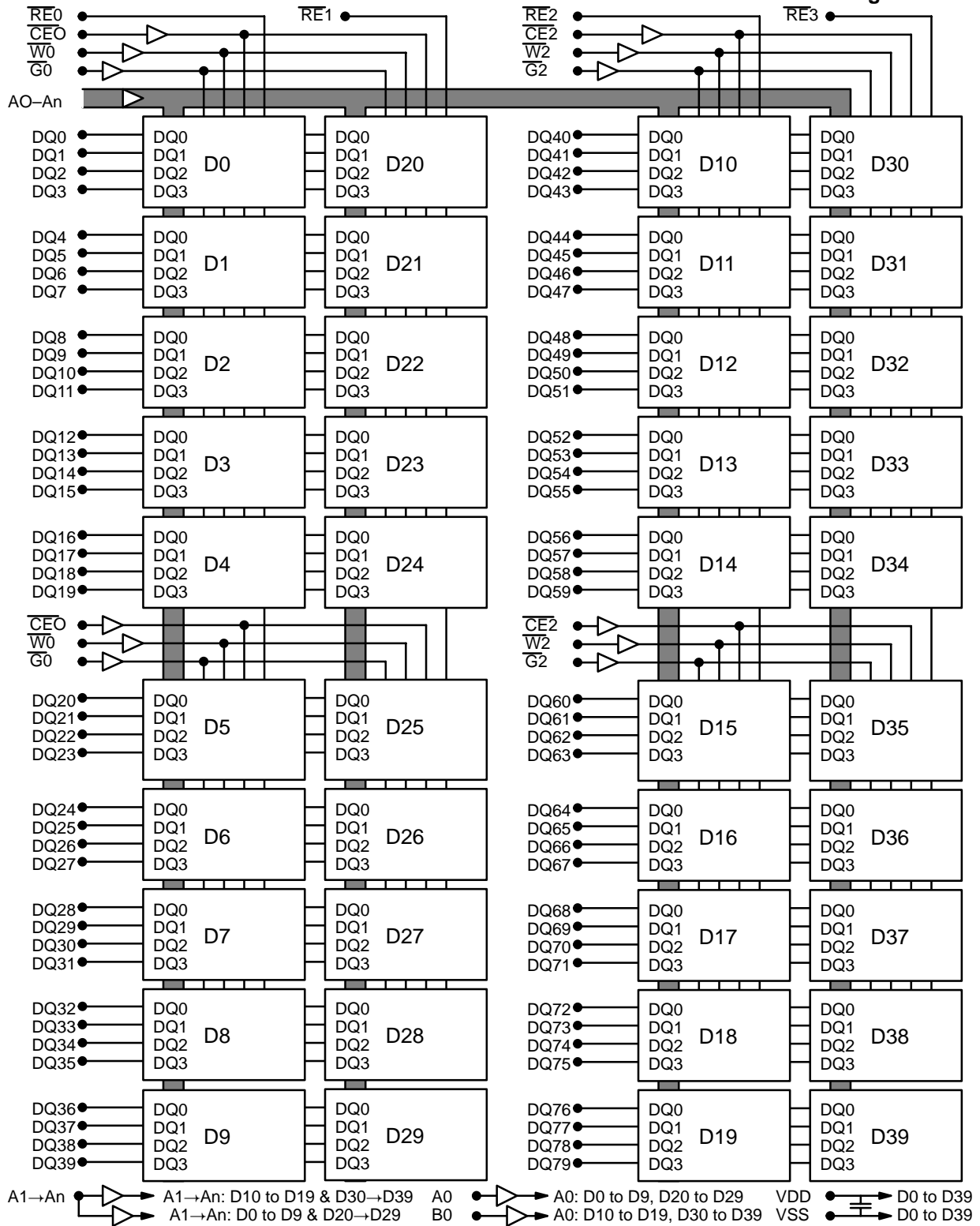


Figure 4.5.1-AB

168 PIN, X80 ECC DRAM DIMM, 2 BANK, X4 DRAMs